Remarks

Claims 1, 4-11, 15-17, 41, 44-55, and 58-68 are pending.

The Examiner rejected Claims 1, 4-8, 10 and 15-17 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,018,178 ("Sung"), in view of U.S. Patent 5,408,115 ("Chang"). With respect to Claim 1, the Examiner states, in pertinent part:

> Thus, Sung is shown to teach all the features of the claim with the exception of alternatively utilizing P-type dopant for the first dopant.
>
> However, Chang teaches that the skill in the art will recognize that while this (the n-channel EEPROM, i.e., p-well, n-type dopant regions) is by far, the most common choice for EEPROM devices, **it is possible to reverse the conductivity and fabricate a p-channel EEPROM array**. (See col. 4, ll. 5-14).
>
> Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the EEPROM of Sung to be p-channel, wherein the first dopant being p-type dopant, as taught by Chang since it is well known in the art to reverse the conductivity dopants to form the similar device, i.e., EEPROM, with difference characteristics, i.e., p-channel and n-channel and vice versa.
>
> Regarding the limitation directing to the functionality or capability of the devices: *the second semiconductor layer and each diffusion region form a junction which is* ***capable of*** *a soft avalanche breadown in response to a lower electrical potential imposed on the diffusion region relative to the second semiconductor layer; the first and second floating gate being* ***capable of*** *storing electrical charge injected into the first or second floating gate in response to the soft avalanche breakdown and a higher electrical potential at the first or second floating gate relative to the first or second diffusion region,* since the device of Sung, in view of Chang, comprises ***all*** physical limitations as claimed, therefore, the device of Sung should be ***capable of*** functioning in the same manner.

Applicants respectfully traverse the Examiner's rejection. Claim 1 recites a P-type memory device formed in a N-type semiconductor layer, which may be programmed using a

soft avalanche breakdown between the semiconductor layer and an associated diffusion region:

1. An electrically alterable memory device, comprising:

a first semiconductor layer doped with a first dopant in a first concentration;

a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;

two spaced-apart diffusion regions embedded in the top side of the second semiconductor layer, each diffusion region being doped with the first dopant in a second concentration greater than the first concentration, the two diffusion regions including a first diffusion region and a second diffusion region with a first channel region defined therebetween, wherein the second semiconductor layer and each diffusion region form a junction which is capable of a soft avalanche breakdown in response to a lower electrical potential imposed on the diffusion region relative to the second semiconductor layer;

a first floating gate comprising a conductive material, the first floating gate being disposed adjacent the first diffusion region and above the first channel region, separated therefrom by a first insulator region, the first floating gate being capable of storing electrical charge injected into the first floating gate in response to the soft avalanche breakdown and a higher electrical potential at the first floating gate relative to the first diffusion region;

a second floating gate comprising a conductive material, the second floating gate being disposed adjacent the second diffusion region and above the first channel region, separated therefrom by a second insulator region, the second floating gate being capable of storing electrical charge injected into the second floating gate in response to the soft avalanche breakdown and a higher electrical potential at the second floating gate relative to the second diffusion region; and

a control gate comprising a conductive material, the control gate being disposed laterally between the first floating gate and the second floating gate, the control gate being separated from the first floating gate by a first vertical insulator layer and being separated from the second floating gate by a second vertical insulator layer, such that the first and second floating gates are each capacitively coupled to have an electrical potential derived from the electrical potential of the control gate, the control gate acting as a word select line, the control gate further being disposed above the first channel region without overlapping the two spaced-apart diffusion regions, being separated therefrom by a third insulator region;

wherein the first dopant has P-type characteristics.

(emphasis added)

The above-underlined limitations are explained in Applicants' Specification, at pages 12-13, paragraph [0036]. In contrast, Sung teaches an N-type device that does not have a diffusion-semiconductor junction subject to a soft avalanche breakdown (See Sung, at col. 4, line 65 to col. 5, line 29). In fact, Sung teaches, at Sung's col. 1, lines 62-67, that Sung's device uses a Fowler-Nordheim injection mechanism to charge the floating gate. As stated by Dr. Simon Wong, in the attached Declaration of Dr. Simon Wong, merely reversing the conductivity of Sung's device would not result in a device that injects charges into the floating gate by a soft avalanche breakdown in the diffusion-semiconductor junction. Thus, Claim 1 recites a device that is neither taught nor suggested by the combined teachings of Sung and Chang. Accordingly, Applicants respectfully submit that Claim 1 and its dependent Claims 4-8, 10 and 15-17, are each allowable over the combined teachings of Sung and Pan. Reconsideration and allowance of Claims 1, 4-8, 10 and 15-17 are therefore requested.

The Examiner rejected Claims 9 and 11 under 35 U.S.C. § 103(a) as being unpatentable over Sung, in view of Chang, and further in view of U.S. Patent 5,760,435

("Pan"), the Examiner citing Pan for teaching either silicon or an O-N-O layer. However, as Claims 9 and 11 each depend from Claim 1, Claims 9 and 11 are each allowable over Sung and Chang for reasons already stated above with respect to Claim 1. Since Pan does not cure the deficiencies of Sung and Chang, Claims 1 and 9 are each allowable over the combined teachings of Sung, Chang and Pan. Reconsideration and allowance of Claims 9 and 11 are therefore requested.

The Examiner rejected Claims 41-48, 50 and 52-54 under 35 U.S.C. § 103(a) as being unpatentable over Sung, in view of U.S. Patent 6,271,089 ("Chen") and Chang. Applicants respectfully traverse the Examiner's rejection. Claim 41 recites a P-type memory device formed in an N-type semiconductor layer, which may be programmed using a soft avalanche breakdown between the semiconductor layer and an associated diffusion region:

> 41. An electrically alterable memory device, comprising:
>
> a first semiconductor layer doped with a first dopant in a first concentration;
>
> a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;
>
> two spaced-apart diffusion regions embedded in the top side of the second semiconductor layer, each diffusion region being doped with the first dopant in a second concentration greater than the first concentration, the two diffusion regions including a first diffusion region and a second diffusion region, with a first channel region defined therebetween, wherein the second semiconductor layer and each diffusion region form a junction which is capable of a soft avalanche breakdown in response to a lower electrical potential imposed on the diffusion region relative to the second semiconductor layer;

a first floating gate having a left side, and a right side and comprising a conductive material, the first floating gate being disposed adjacent the first diffusion region and above the first channel region and being separated therefrom by a first insulator region, the first floating gate being capable of storing electrical charge injected into the first floating gate in response to the soft avalanche breakdown and a higher electrical potential at the first floating gate relative to the first diffusion region;

a second floating gate having a left side, and a right side and comprising a conductive material, the second floating gate being disposed adjacent the second diffusion region and above the first channel region, being separated therefrom by a second insulator region, the second floating gate being capable of storing electrical charge injected into the second floating gate in response to the soft avalanche breakdown and a higher electrical potential at the second floating gate relative to the second diffusion region; and

a control gate comprising a conductive material, the control gate being disposed laterally between the first floating gate and the second floating gate, the control gate being separated from the first floating gate by a third insulator layer and being separated from the second floating gate by a fourth insulator layer, such that the first and second floating gates are each capacitively coupled to have an electrical potential derived from the electrical potential of the control gate, the control gate covering the first floating gate on at least right side and left side, the control gate further covering the second floating gate on at least right side and left side, the control gate further being disposed above the first channel region and separated therefrom by a third insulator region;

wherein the first dopant has P-type characteristics.

(emphasis added)

The above-underlined limitations are explained in Applicants' Specification, at pages 12-13, paragraph [0036]. In contrast, Sung teaches an N-type device that does not have a diffusion-semiconductor junction subject to a soft avalanche breakdown (See Sung, at col. 4,

line 65 to col. 5, line 29). In fact, Sung teaches, at Sung's col. 1, lines 62-67, that Sung's device uses a Fowler-Nordheim injection mechanism to charge the floating gate. Chen does not cure Sung's deficiency (e.g., Chen also teaches at Figure 1, and at col. 1, lines 26-40, an N-type device). As stated by Dr. Simon Wong, in the attached Declaration of Dr. Simon Wong, merely reversing the conductivity of Sung's device would not result in a device that injects charges into the floating gate by a soft avalanche breakdown in the diffusion-semiconductor junction. Therefore, Claim 41, and its dependent Claims 44,-48, 50 and 52-54 are each allowable over the combined teachings of Sung and Chen. Reconsideration and allowance of Claim 41 and its dependent Claims 44-48, 50 and 52-54 are requested.

The Examiner rejected Claims 49 and 51 under 35 U.S.C. § 103(a) as being unpatentable over Sung and Chen, as applied to Claim 41, and further in view of Pan. Although the Examiner did not mention Chang in this statement rejection, because the Examiner rejected parent claim 41 based on combining the teachings of Sung, Chen and Chang, Applicants assume that the Examiner's rejection of Claims 49 and 51 is based on Sung, Chen, Chang and Pan. As Claims 49 and 51 each depend from Claim 41, Claims 49 and 51 are each allowable over the combined teachings of Sung, Chen and Chang for the reasons discussed above. As the Examiner merely cites Pan for teaching using ONO as an insulator material, the combined teachings of Sung, Chen, Chang and Pan neither disclose nor suggest Applicants' Claims 49 and 51. Reconsideration and allowance of Claims 49 and 51 are therefore requested.

The Examiner rejected Claims 55-68 under 35 U.S.C. § 103(a) as being unpatentable over Sung, in view of U.S. Patent 5,576,232 ("Hong") and Chang. Applicants respectfully traverse the Examiner's rejection. Claim 55 recites a P-type memory device formed in an N-

type semiconductor layer, which may be programmed using a soft avalanche breakdown between the semiconductor layer and an associated diffusion region:

55. An electrically alterable memory device, comprising:

a first semiconductor layer doped with a first dopant in a first concentration;

a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;

two spaced-apart diffusion regions embedded in the top side of the second semiconductor layer, each diffusion region being doped with the first dopant in a second concentration greater than the first concentration, the two diffusion regions including a first diffusion region and a second diffusion region, with a first channel region defined therebetween, wherein the second semiconductor layer and each diffusion region form a junction which is capable of a soft avalanche breakdown in response to a lower electrical potential imposed on the diffusion region relative to the second semiconductor layer;

a first floating gate comprising a conductive material, the first floating gate being disposed adjacent the first diffusion region and above the first channel region and being separated therefrom by a first insulator region, the first floating gate being capable of storing electrical charge injected into the first floating gate in response to the soft avalanche breakdown and a higher electrical potential at the first floating gate relative to the first diffusion region;

a second floating gate comprising a conductive material, the second floating gate being disposed adjacent the second diffusion region and above the first channel region, being separated therefrom by a second insulator region, the second floating gate being capable of storing electrical charge injected into the second floating gate in response to the soft avalanche breakdown and a higher electrical potential at the second floating gate relative to the second diffusion region; and

a control gate having at least two lateral sides and comprising a conductive material, the control gate being disposed laterally between the first floating gate and the second floating gate, the control gate being separated from the first floating gate by a first vertical insulator layer and being separated from the second floating gate by a second vertical insulator layer, such that the first and second floating gates are each capacitively coupled to have an electrical potential derived from the electrical potential of the control gate, the control gate being covered by the first floating gate on more than one lateral side and being covered by the second floating gate on more than one lateral side, the control gate being separated from the first channel region by a third insulator region;

wherein the first dopant has P-type characteristics.

The above-underlined limitations are explained in Applicants' Specification, at pages 12-13, paragraph [0036]. In contrast, Sung teaches an N-type device that does not have a diffusion-semiconductor junction subject to a soft avalanche breakdown (See Sung, at col. 4, line 65 to col. 5, line 29). In fact, Sung teaches, at Sung's col. 1, lines 62-67, that Sung's device uses a Fowler-Nordheim injection mechanism to charge the floating gate. Hong does not cure Sung's deficiency (e.g., Hong also teaches at Figures 7a-7h, and at col. 5, lines 11-41, an N-type device). As stated by Dr. Simon Wong, in the attached Declaration of Dr. Simon Wong, merely reversing the conductivity of Sung's device would not result in a device that injects charges into the floating gate by a soft avalanche breakdown in the diffusion-semiconductor junction. Therefore, Claim 55, and its dependent Claims 54-68 are therefore each allowable over the combined teachings of Sung, Hong and Chang. Reconsideration and allowance of Claim 55 and its dependent Claims 58-68 are requested.

Therefore, for the reasons set forth above, all pending claims (i.e., Claims 1, 4-11, 15-17, 41, 44-55 and 58-68) are allowable over the art of record. If the Examiner has any

question regarding the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant at 408-392-9250.

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